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328654(28)

B. E. (Sixth Semester) Examination Nov.-Dec. 2021

(New Scheme)

(Et&T Branch)

VLSI DESIGN

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : *Attempt all questions. Part (a) of each question is compulsory. Attempt any two parts from (b), (c) and (d) each question. Colors are allowed to make stick diagram and layout.*

Unit-I

1. (a) What is Moore's Law? 2

   (b) Explain VLSI design flow. 7

(c) Explain the switching characteristics of CMOS inverter. 7

(d) Explain Transmission gate. Design Multiplexer with transmission gate. 7

Unit-II

2. (a) What is Lithography? 2

(b) What are the fabrication processes for *n*-well CMOS? 7

(c) Draw layout and stick diagram of 2 input NOR gate. 7

(d) Explain Euler Graph with an example. 7

Unit-III

3. (a) What are SRAM and DRAM? 2

(b) Draw layout of SR-Flip Flop. 7

(c) Draw schematic and layout of multiplexer. 7

(d) Explain the working of a 4 × 4 NOR based ROM array and draw its layout. 7

Unit-IV

4. (a) Define PAL and PLA. 2

(b) Compare VLSI design style with FPGA and CPLD. 7

(c) Explain concurrent and sequential signal Assignment with an example. 7

(d) Write a VHDL code for Encoder. 7

Unit-V

5. (a) What is sequential circuits? 2

(b) Write VHDL code to detect the sequence "101" using Moore State Machine. 7

(c) Write VHDL code for D type Flip Flop with synchronous and asynchronous clear. 7

(d) What is test bench synthesis? Explain with an example. 7